2nd International Conference on Electrical and Electronics Engineering (ICEEE) and XI Conference on Electrical Engineering (CIE 2005)
Mexico City, Mexico. September 7-9, 2005

On the design of an FPGA-Based OFDM modulator for IEEE 802.11a

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Abstract — **The actual and next communication schemes tend to use OFDM systems in order to provide high baud rates and less inter symbol interference. Some examples are 802.11, 802.16, MC-CDMA, Digital Video Broadcasting, Wireless USB or Wireless Firewire among others. Trying to provide a solution to the new devices emerging, slow standard adoption, poor spectrum use, etc. Joe Mitola introduced the concept of "Software Defined Radio", which involves exhaustive configurable digital signal processing like FFT, therefore FPGAs could support many of its operations. This work presents a FPGA design, validation and implementation of an "Orthogonal Frequency Division Multiplexing" (OFDM) modulator for IEEE 802.11a using a high level design tool, also reports the resources requirements for the presented system.**

Keywords — **OFDM, FPGA, 802.11, SDR.**

I. Introduction

Orthogonal Frequency Division Multiplexing (OFDM) could be tracked to 1950's but it had become very popular at these days, allowing high speeds at wireless communications [1]. OFDM could be considered either a modulation or multiplexing technique, its hierarchy corresponds to the physical and medium access layer. A basic OFDM system consists of a QAM or PSK modulator/demodulator, a serial to parallel / parallel to serial converter, and an IFFT/FFT module. The iterative nature of the FFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. Using FPGA instead of an ASIC gives also flexibility for reconfiguration, which is a need for the Software Defined Radio (SDR) concept. The focus of this work is to validate the suitability of reconfigurable devices such as FPGAs to perform IF "Intermediate Frequency" processing to support SDR [2]. This work presents the mapper, interleaver, IFFT and prefix adding modules for a Std. 802.11a compliant OFDM modulator FPGA implementation using a high-level design tool.

Present work is divided as follows: Section II presents the related work; section III presents a brief description of the Std. IEEE 802.11 and OFDM fundamentals; at section IV the block diagram, the explanation of each block as the system design are presented; section V is dedicated to results and finally at section VI conclusions are discussed.

II. Related work.

Moisés Serra [3] shows the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan/2 based, the features of that transmitter are: 36 Mbit/s, ¾ punctured code rate, 16QAM, 64-IFFT and cyclic prefix of 16 samples, meanwhile this work presents all the QAM and PSK alphabets supported by the Std. IEEE 802.11a. [3] is a very similar work to the one presented here, the work presented by M. Serra et al. uses System generator as well as this work does; contrasting Ma. José Canet [4] shows implementation issues of a digital transmitter for an OFDM based WLAN systems and benchmarks some optimized VHDL area results against System Generator results, Canet's work is focused on the solutions for the OFDM signal generation in base-band and in intermediate frequency (IF).

Chris Dick [5] emphasizes the suitability of high-level design tools when designing sophisticated systems, and the importance to design FPGA systems rather than ASIC to one day accomplish the SDR "Software Defined Radio" concept and gives a high-level overview of the FPGA implementation giving some deep to the synchronization, packet detection, preamble correlator channel estimation and equalization; that is mainly at the OFDM receiver.

There are few reported works about a complete FPGA transmitter for an OFDM schema; Ludovico de Souza et. al. [6] present a FPGA implementation capable to support 802.11 wireless modems but just as a validating and prototyping stage for an ASIC, that work do not focus on the suitability of FPGA to perform IF processing. Contrasting this philosophy Youjim Kim et al. [7] report a MAC implementation for IEEE 802.11 wireless LAN, which supports not only OFDM but DSSS "Direct Sequence Spread Spectrum", using a combination of FPGA and ARM7 core, showing a pretty HW/SW co-design.

This work is focused on the FPGA suitability to support IF processing for the Std. IEEE 802.11a and the resource area and timing requirements either for rapid prototyping or to take advantage of re-configurability in order to be able to support different standards, where this work reports better results than the OFDM Demonstrator [3]. Estimated power consumption is also presented.

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2
0-7803-9230-2/05/$20.00 ©2005 IEEE.

III. 802.11 & OFDM OVERVIEW

A. The Standard IEEE 802.11

Standard 802.11 [8] also known as ISO/IEC DIS 8802-11 is part of a family of standards for local and metropolitan area networks Std IEEE 802. The standard IEEE 802.11 covers the Wireless LAN Medium Access Control and Physical Layer Specifications.

802.11a specifies OFDM as the multiplexing and modulation technique for the wireless LANs supporting this standard, which covers the physical and medium access specifications. Some of the specified aspects of the standard are IFFT/FFT of 64 points where 48 of the sub-carriers are used to carrier data from BPSK, QPSK, 16-QAM or 64-QAM alphabet; four pilot signals are added to the sub-carriers, for phase tracking, then the symbol is zero padded to complete the 64 points after IFFT module 16 point cyclic prefix is added to have a complete OFDM symbol (80 points); the OFDM symbol's period is 4 s, while an IFFT symbol duration is 3.2 s, that is a rate of 4/5 which uses to be a health rate for OFDM systems [9]. At the following section is given a brief description of OFDM which is the one employed by 802.11, but not limited to this standard.

B. OFDM Fundamentals

OFDM is a special case of multi-carrier transmission, where a single data stream is transmitted over a number of lower rates sub-carriers. On classical frequency division multiplexing the total band is divided into N non-overlapping frequency channels, while on OFDM the band is divided into a number of overlapping frequency channels [9] but with orthogonal frequencies, the consequence is a better use of the available spectrum. Those orthogonal frequencies could be achieved by the IFFT. As described at Std. IEEE 802.11a [5] the OFDM Physical layer (PHY) transmitter blocks are: FEC Coder, Interleaving/Mapping, IFFT, Guard Interval (Cyclic Prefix), In Phase and Quadrature Modulation (IF) and finally the RF modulation. Those blocks as specified by IEEE 802.11a are shown at Fig. 1.

IV. SYSTEM DESIGN FLOW.

It was mentioned before a high-level design tool was used, Xilinx System Generator which runs under MatLab Simulink, a visual modeling tool. This tool allows a high level abstraction of the system. Not only design was performed by System Generator but verification and finally targeting to a specific FPGA. This work divides the design into functional subsystems: PSK or QAM mapping, pilot generator, inter-leaver which mix all sources (mapped data, pilots and zero pads), IFFT and prefix adding.

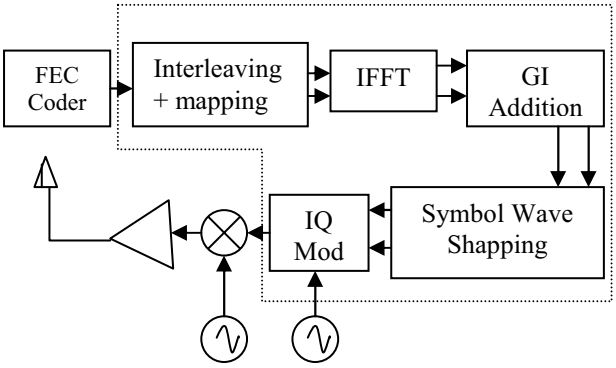

Fig. 1. 802.11a Transmitter block diagram for the OFDM PHY.

Regarding the frequency of operation, this design uses an 80 MHz for the main clock which is down-sampled to obtain a 16 MHz, used before IFFT block and 20 MHz after IFFT block. All blocks use a 10 bits signed fixed point representation, but IFFT uses 16 bit resolution. The decision of using 10 fixed point bits was supported on the work presented by Gifford [10].

A. PSK or QAM mapping

This block consist of a number of ROMs containing the constellation mapping for each of the specified modulation schemes (BPSK, QPSK, 16-QAM and 64-QAM), two multiplexers which selects the In Phase and Quadrature data from the desired modulation scheme stored on ROMs. Finally the data is stored on a FIFO component to pass to next stage, as shown at Fig. 2.

B. Inter-leaver.

Inter-leaver block combines data, pilots and zero pads. The structure for the IFFT input must be {5 samples data, a pilot, 13 samples data, a pilot, 6 samples data, a zero, 6 samples data, a pilot, 13 samples data, a minus pilot, 5 samples data, 11 zeros}. Then the function of this block is to interleave data, pilots and zeros as described by the mentioned structure. For this purpose a counter is used to know which input turn is, then using a combinational logic a multiplexer is selected to take data, pilot or zero according to its position (given by the counter). This model is shown at Fig. 3.

C. IFFT and prefix adding

IFFT uses a radix-4 butterfly since it is and Xilinx IP core, however parallel butterfly algorithms are the most suitable for OFDM [11]. The IFFT receives the inter-leaved data at 16 MHz, but the IFFT Xilinx IP Core receives data at 3 times its clock which is the main one of 80 MHz, for this reason the incoming data is up-sampled by 5 and then down-sampled by 3, thus additional logic is required to mark the data as valid or not, and then passing it to the IFFT block.

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2

The IFFT block takes 192 cycles to perform the transform (2.4 s), the results are stored into four FIFO blocks; two of them store the real and imaginary coefficients of the 64 points transform; the other two FIFO stores the last 16 real and imaginary coefficients that will be used as the cyclic prefix, in order to have an 80 points symbol at the end. The model architecture for this module is shown at Fig. 4.

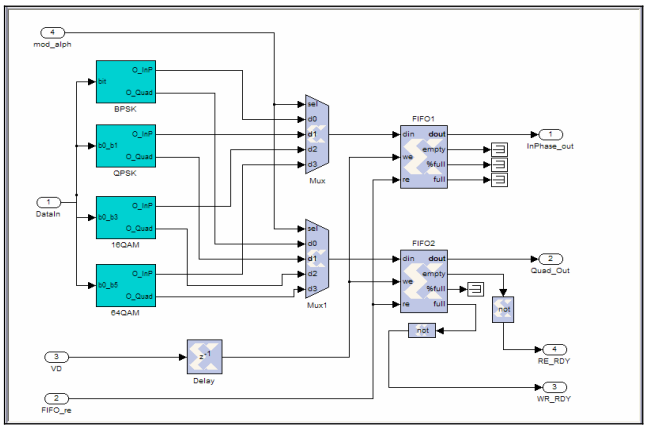

Fig. 2. PSK or QAM mapping model.

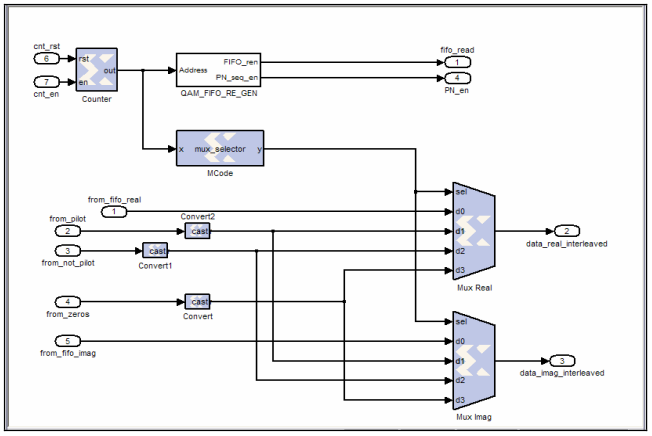

Fig. 3. Inter-leaver model.

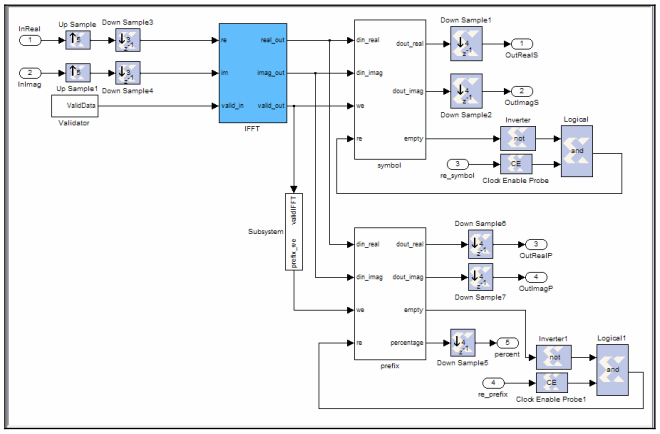

Fig. 4. IFFT and prefix adding model.

V. Results.

Once the model was completed, its conformance with Sdt 802.11a [8] could be validated by running a simulation at MatLab. The use of this high level tool simplifies all prototyping process contrasting a VHDL test bed validation approach which would require more prototyping time and effort.

During simulations all specified modulation schemes (BPSK, QPSK, 16-QAM and 64-QAM) were tested at base band frequency (20 MHz), no channel model were used, neither DDS or DDC were performed at this time.

The model was targeted to a Virtex 2 xc2v3000-4fg676, the result was that all mentioned modules requires around 10% of the available resources, while the Maximum Frequency estimated was almost 92 MHz, which is enough for the requirement of 80 MHz architecture to generate 20 MHz (OFDM Symbol frequency specified at 802.11a) and 16 MHz clocks. Detailed area, and timing results are shown at tables 1and 2. These results were obtained using Xilinx´s ISE 6.3i tool.

TABLE I
AREA RESULTS

Area metrics for a XC2V3000-4FG676 device		
Parameter	**Used**	**%**
Number of Slices	1678	11
Number of Slice Flip Flops	2353	8
Number of 4 input LUTs	2814	9
Number of bonded IOBs	29	5
Number of BRAMs	12	12
Number of GCLKs	1	6

TABLE II
TIMING RESULTS

Timing metrics for a XC2V3000-4FG676 device	
Parameter	**Time (ns) Frequency (MHz)**
Minimum Period	10.876
Maximum Frequency	91.948
Minimum input arrival time before clock	4.374
Maximum output required time after clock	6.973

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2

Estimated power consumption for this architecture is 9.06 mW/MHz according to the estimates provided by Xilinx's XPower tool. The work presented at [3] is very similar to this and evaluated on a Virtex XCV300 that work uses 2806 slices, this work just 1678. [3] takes 3075 flip-flops, this work just 2353; [3] uses 2676 LUTs and this work, just a little more, 2814 finally both works, [3] and this one, take 12 block RAMs. To be fair this work was synthesized for XCV300 with the following results: 1924 slices, 2367 flip flops, 2500 LUTs and 12 block RAMs. Summarizing, this work, employs less area resources than the OFDM Demonstrator at [3].

Now compare some particular modules with other works. This work IFFT takes 192 cycles to perform the transform while the ASIC DSP proposed at [12] takes 392. The results from the IFFT are buffered to a dual port memory at [5], this work uses a FIFO structure to store results and cyclic prefix which is a simple way to produce the prefix adding stage.

VI. Conclusion

It has been presented the complete design, validation and implementation of an OFDM modulator compliant with the Std. IEEE 802.11a. This work was performed using high-level tools like System Generator and modeling tools as MatLab & Simulink that facilitate this task.

The result presented shown that is possible to implement an OFDM modulator for IEEE Std. 802.11a using an available device like Virtex 2 (using around 10 % of the available resources). These results show that actual devices could support the SDR concept at IF processing level even at high arithmetic demanding standards or process.

This work requires fewer resources than the required by a similar work presented by M. Serra [3]; and it is feasible to reduce more resources using VHDL optimizing techniques like the work presented by M. Canet [4], however that optimization would require much more time than using a high level tool.

Future work includes the demodulator modeling as well other standards like IEEE 802.16.

Acknowledgment

This work has been partially supported by CONACyT "National Council for Science and Technology" of Mexico under grant number 181689.

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